IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor memory device, comprising:

a plurality of memory mats arranged in a bit-line direction ~~of bit-line~~ which ~~including~~includes bit lines, word lines and memory cells coupled to said bit lines and said word lines;

a MOSFET included in each of said memory cells and having a capacitance having first and second electrodes, a gate coupled to a corresponding one of said word lines and source-and-drain paths, one of which is coupled to a corresponding one of said bit lines and the other of which is coupled to said first electrode of said capacitance; and

a sense amplifier array provided in a region between said memory mats arranged in a direction of said bit line and having latch circuits having input/output nodes connected to a half ~~number~~ of the bit line pairs provided to each of said memory mats,

wherein a failed bit line of said bit line pairs can be replaced, on a bit-line basis, with a redundant bit line and a corresponding redundant sense amplifier.

2. (Original) A semiconductor memory device according to claim 1, wherein said failed bit line is failed due to the presence of a failure on said memory cell itself.

3. – 13. (Cancelled)

14. (Currently Amended) A semiconductor memory device, including:

a first bit line;

a second bit line;

a first redundant bit line;

a second redundant bit line;

a plurality of first memory cells connected to said first bit line;

a plurality of second memory cells connected to said second bit line;

a plurality of first redundant memory cells connected to said first redundant bit line;

a plurality of second redundant memory cells connected to said second redundant bit line;

a first amplifier circuit connected to said first bit line and said second bit line to amplify a difference of potential between said first bit line and said second bit line; and

a first redundant amplifier circuit connected to said first redundant bit line and said second redundant bit line to amplify a difference of potential between said first redundant bit line and said second redundant bit line,

wherein said first bit line is to be replaced with said first redundant bit line but said second bit line is not to be replaced with said second redundant bit line.

15. (Currently Amended) A semiconductor memory device according to claim 14, wherein said first bit line and said first redundant bit line are included in a first memory array,

said second bit line and said second redundant bit line ~~are~~being included in a second memory array, and

said first amplifier circuit and said first redundant amplifier circuit being formed in a region between said first memory array and said second memory array.

16. (Original) A semiconductor memory device according to claim 15, wherein said second memory array further includes a third bit line,

said semiconductor memory device further including a third memory array including a fourth bit line and a second amplifier circuit connected to said third bit line and said fourth bit line to amplify a potential difference between said third bit line and said fourth bit line; and

said second amplifier circuit being formed in a region between said second memory array and said third memory array.

17. (Original) A semiconductor memory device according to claim 14, wherein said first bit line, said second bit line, said first redundant bit line and said second redundant bit line are included in said first memory array,

said first bit line and said second bit line being arranged in parallel; and

said first redundant bit line and said second redundant bit line being arranged in parallel.

18. (Currently Amended) A semiconductor memory device according to claim 17, wherein said first memory array further ~~including~~includes a third bit line and a fourth bit line,

said semiconductor memory device further including a second amplifier circuit connected to said third bit line and said fourth bit line to amplify a potential difference between said third bit line and said fourth bit line;

said first amplifier circuit and said first redundant amplifier circuit being formed in a first region;

said second amplifier circuit being formed in a second region; and

said first memory array being formed in a region between said first region and said second region.

19. (Original) A semiconductor memory device according to claim 14, wherein said first bit line, said second bit line, said first redundant bit line and said second redundant bit line are included in a first memory array.

20. – 28. (Cancelled)

29. (Original) A semiconductor memory device, including:

a plurality of first normal bit lines;

a plurality of second normal bit lines;

a first redundant bit line;

a second redundant bit line;

a plurality of first normal memory cells connected to said plurality of first normal bit lines;

a plurality of second normal memory cells connected to said plurality of second normal bit lines;

a plurality of first redundant memory cells connected to said first redundant bit line;

a plurality of second redundant memory cells connected to said second redundant bit line;

a plurality of first amplifier circuits connected to said plurality of first bit lines and said plurality of second bit lines;

a second amplifier circuit connected to said first redundant bit line and said second redundant bit line to amplify a potential difference between said first redundant bit line and said second redundant bit line; and

an information hold circuit which holds information about replacement of a normal bit line ~~into~~with a redundant bit line,

wherein each of said first amplifier circuits amplifies a potential difference between a corresponding one of said first normal bit lines and a corresponding one of said second normal bit lines~~;~~,

said information hold circuit replacing one of said first normal bit lines ~~into~~with said first redundant bit line but not replacing one of said second normal bit lines corresponding to said one of said first normal bit lines ~~into~~with said second redundant bit line.

30. (Currently Amended) A semiconductor memory device according to claim 29, wherein said information hold circuit can hold information to replace one of said second normal bit lines ~~into~~with said second redundant bit line but not to replace one of said first normal bit lines corresponding to said one of said second normal bit lines ~~into~~with said first redundant bit line.

31. (Currently Amended) A semiconductor memory device according to claim 29, wherein said information hold circuit can hold information that one of said first normal bit lines is to be replaced ~~into~~with said second redundant bit line and one of said second normal bit lines ~~into~~with said first redundant bit line.

32. (Currently Amended) A semiconductor memory device according to claim 29, wherein said information hold circuit can hold information that one of said first normal bit lines connected to one of said first amplifier circuits and one of said second normal bit lines are to be respectively replaced ~~into~~with said first redundant bit line and said second redundant line.

33. (Curretly Amendede) A semiconductor memory device according to claim 29, wherein said information hold circuit can hold information that one of said first normal bit lines connected to one of said first amplifier circuits is to be replaced ~~into~~with said first redundant bit line and one of said second normal bit lines connected to another of said first amplifier circuits is to be replaced ~~into~~with said second redundant bit line.